WHAT IS CLAIMED IS:

1. A design support system comprising:

an information merging section for capturing semiconductor chip information and lead frame information, and for generating semiconductor chip and lead frame merged information for individual semiconductor chips;

a connection information generating section for generating connection information between the semiconductor chips and lead frame for the individual semiconductor chips from the semiconductor chip and lead frame merged information generated by said information merging section; and

an inter-semiconductor chip and lead frame connection information integrating section for generating integrated connection information between the semiconductor chips and the lead frame from the connection information between the semiconductor chips and the lead frame generated by said connection information generating section, the integrated connection information enabling the entire connection information between the semiconductor chips and lead frame to be displayed on a single drawing.

2. The design support system according to claim 1, further comprising a recording section for recording at least one of the semiconductor chip information, lead frame information, the connection information between the semiconductor chips and lead frame and the integrated connection information between the semiconductor chips and the lead frame.

3. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a display type selection function allowing to select colors and shades of gray when producing a drawing.

4. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a semiconductor chip selection function allowing to select an arbitrary semiconductor chip when producing a drawing.

5. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a semiconductor chip group layer selection function allowing to select an arbitrary semiconductor chip group consisting of a plurality of semiconductor chips when producing a drawing.

6. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a forward/reverse rotation selection function allowing to select forward/reverse rotation of the individual semiconductor chips when producing a drawing.

7. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame

connection information integrating section has a component selection function allowing to select an arbitrary component when producing a drawing.

8. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a display rescaling function allowing to changing a scaling factor of any specified region when producing a drawing.

9. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a 3-D display function allowing to carry out 3-D display of any specified region when producing a drawing.

10. The design support system according to claim 8, wherein said inter-semiconductor chip and lead frame connection information integrating section has a rotating function allowing to rotate, by any specified angle, the integrated connection information between the semiconductor chips and the lead frame, which is displayed by using at least one of a display rescaling function and a 3-D display function.

11. The design support system according to claim 9, wherein said inter-semiconductor chip and lead frame connection information integrating section has a rotating function allowing to rotate, by any specified angle, the integrated connection information between the

semiconductor chips and the lead frame, which is displayed by using at least one of a display rescaling function and a 3-D display function.

12. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a simplified display function allowing to carry out simplified display of the integrated connection information between the semiconductor chips and the lead frame.

13. The design support system according to claim 1, further comprising a recording section for recording simplified display information, wherein said information merging section captures the semiconductor chip information, the lead frame information and the simplified display information, and generates semiconductor chip and lead frame merged information for individual semiconductor chips.

14. The design support system according to claim 1, wherein said inter-semiconductor chip and lead frame connection information integrating section has a connection wire number verification function of counting a number of connection wires that are connected to each semiconductor chip.

15. The design support system according to claim 1, further comprising a print data generating section for

generating print data from the integrated connection information between the semiconductor chips and the lead frame; and a drawing data generating section for generating drawing data from the integrated connection information between the semiconductor chips and the lead frame.

16. A design support method comprising:

an information merging step of capturing semiconductor chip information and lead frame information, and generating semiconductor chip and lead frame merged information for individual semiconductor chips;

a connection information generating step of generating connection information between the semiconductor chips and lead frame for the individual semiconductor chips from the semiconductor chip and lead frame merged information; and

an inter-semiconductor chip and lead frame connection information integrating step of generating integrated connection information between the semiconductor chips and the lead frame from the connection information between the semiconductor chips and the lead frame, the integrated connection information making it possible to display the entire connection information between the semiconductor chips and lead frame in a single drawing.

17. The design support method according to claim 16, wherein the information merging step captures the semiconductor chip information, the lead frame

information and simplified display information, and generates the semiconductor chip and lead frame merged information for individual semiconductor chips.

18. The design support method according to claim 16, further comprising a print data generating step of generating print data from the integrated connection information between the semiconductor chips and the lead frame; and a drawing data generating step of generating drawing data from the integrated connection information between the semiconductor chips and the lead frame.